Improvement of Conversion Gain and Pixel Linearity through Source Follower Drain Design in CMOS image sensors

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Abstract— In this study, we investigate the characteristics of CMOS image sensors with respect to the reduction in the drain width of the Source Follower (SF) transistor. Compared to conventional SF transistors with equal source and drain widths, we varied the drain width and explored its effects. The reduction in drain width was proposed to efficiently decrease the SF capacitance and reduce the short-channel effect. Our results show that as the drain width decreases, the SF transistor capacitance relative to the area significantly reduces. Specifically, when the drain width is reduced to 33% of its original size, the ratio of SF capacitance to area decreases to approximately 88% of the corresponding ratio in the conventional SF transistor. This reduction provides a significant advantage in terms of achieving a higher Conversion Gain within the same area, when compared to conventional SF transistors. Furthermore, as the drain width decreases, the short-channel effect improves. In the Test Element Group (TEG) measurements, the reduction in drain width resulted in a decrease of approximately 50% compared to the conventional SF transistor. Additionally, the low-light signal non-linearity was improved by about 54%. We believe that optimal width control in Source Follower design is essential and anticipate that it will make a significant contribution to the improvement of CMOS image sensor (CIS) characteristics.

Keywords—CMOS Image Sensors, Source follower Transistor, Random noise, Conversion Gain, Signal non linearity

I. INTRODUCTION

The CMOS image sensor (CIS) industry has made significant progress toward the development of pixels with a higher signal-to-noise ratio (SNR), which is a crucial factor in enhancing image quality, particularly in challenging conditions such as low-light environments. To improve SNR in such conditions, minimizing input-referred noise is essential [1,2]. This can be effectively achieved by increasing the conversion gain (CG), which is inversely related to the total capacitance of the floating diffusion (FD). A lower FD capacitance leads to a higher conversion gain (CG), thereby reducing noise and improving overall image quality. The source follower transistor (SF Tr.) plays a key role in determining the FD capacitance, significantly affecting factors such as random noise, random telegraph signal (RTS), and the linearity of CIS performance [3]. While increasing the SF Tr. area can improve the overall electrical characteristics of the sensor, it simultaneously reduces the CG, which may lower the SNR, especially in low-light conditions. Therefore, careful and precise consideration of the SF Tr. dimensions is essential to achieve a balance between enhanced electrical characteristics and minimal noise, ensuring optimal CIS performance.[4]

In this work, we propose a CIS integrating a narrow drain SF transistor (NDSF Tr.), which reduces the drain width relative to the source width to improve CG and overcome linearity degradation caused by short-channel effects

II. EXPERIMENT AND RESULT

We fabricated a 4-transistor active pixel sensor as shown in Figure 1(a), and the diagram and capacitances of the SF transistor are shown in Figures 1(b) and 1(c).

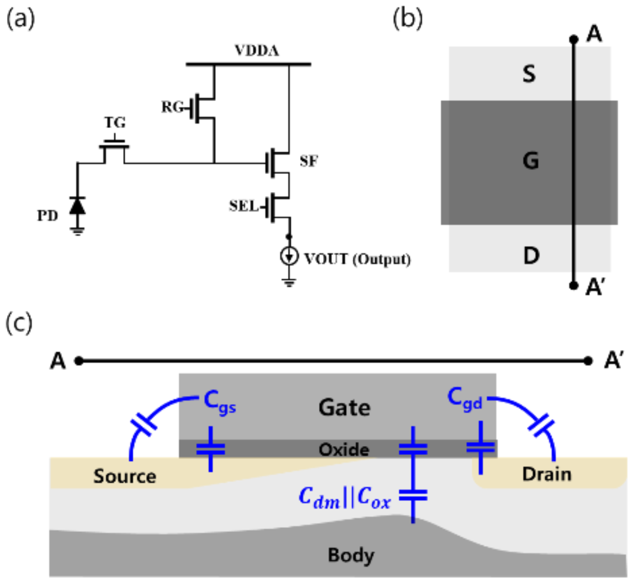

Figure 1. 4T CMOS Image Sensors

a) schematic b) conventional SF Tr. top view c) conventional SF Tr. cross-sectional view

The equation describing the SF transistor capacitance is provided in Equation 1.

$$SF\ cap = C_{gs} + C_{dm}||C_{ox} + C_{gd}$$

$$= (\tfrac{2}{3}WLC_{ox} + WC_{ov}) * (1 - Av) + ((\tfrac{1}{3}WL\left(\frac{SS}{60mV} - 1\right)C_{ox})||(\tfrac{1}{3}WLC_{ox})) + WC_{ov}$$

- Equation 1.

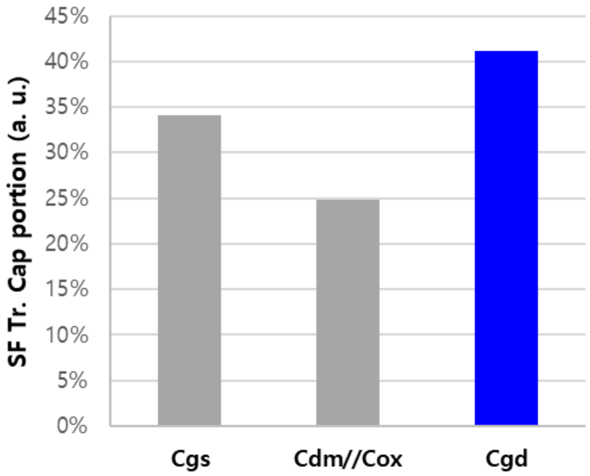

Figure 2. Capacitance ratio of conventional SF Tr. gate-to-source capacitance (C_{gs}), gate-to-body capacitance ($C_{dm}||C_{dm}$), gate-to-drain capacitance (C_{gd})

As seen in Figure 2, the drain capacitance is the largest contributor to the total capacitance, and it can be reduced with minimal impact on the SF Tr. area.

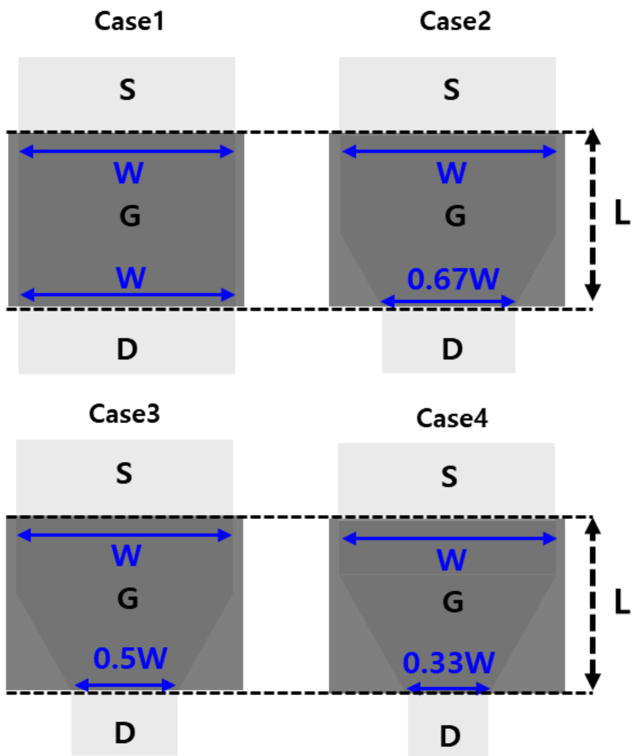

Figure 3. Conventional SF Tr. (Case1), NDSF Tr. illustration with varying drain width (Case2~4)

The NDSF Tr. design is presented in Figure 3. Case 1 represents the conventional SF Tr., while Cases 2 through 4 illustrate NDSF Tr. with varying drain widths. The source width and length are consistent across all cases. Figure 4 shows the SF capacitance composition ratios for each case. As the drain width decreases, the area-related capacitance reduces less, while the overlap capacitance (C_{ov}) decreases proportionally. Table 1 presents the SF area, CG, input-referred noise, and RTS characteristics for each case. By adopting NDSF Tr., CG increases and input-referred noise decreases. Furthermore, even in cases where the area is kept constant, such as in Case 3 and Case 4, an increase in CG can be achieved by reducing the drain width. Thus, the NDSF Tr. enables efficient control of the capacitance ratios that contribute to the SF capacitance.

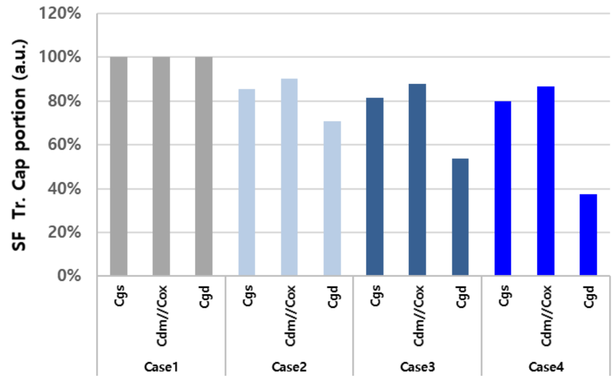

Figure 4. Comparison of capacitance ratios for each case of SF Tr.

	Case1	Case2	Case3	Case4
SF Area	**100%**	**87%**	**84%**	**84%**
C.G	**100%**	**104%**	**105%**	**106%**
Input-referred noise	**100%**	**99%**	**98%**	**97%**
RTS	**100%**	**110%**	**130%**	**135%**

Table 1. Comparison of SF Area, C.G, input referred noise, RTS for each case

As shown in Figure 5, Conventional Tr. exhibits a linear decrease in SF Tr. Cap with the reduction of S/D width, while NDSF Tr. can achieve a variety of Cap reductions depending on changes in the Drain Width design. In other words, as shown in Figure 6, the NDSF Tr. exhibits 88% of the capacitance of the conventional SF Tr. when considering the area. Moreover, when comparing the conventional SF Tr. and the NDSF Tr. with the same area, the NDSF Tr. demonstrates a higher CG.

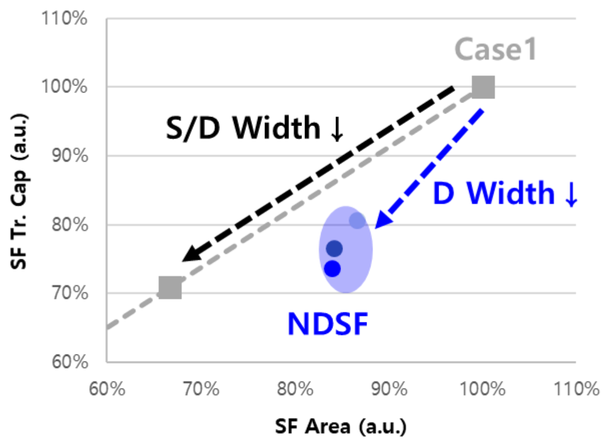

Figure 5. Relationship between SF Tr. capacitance and area

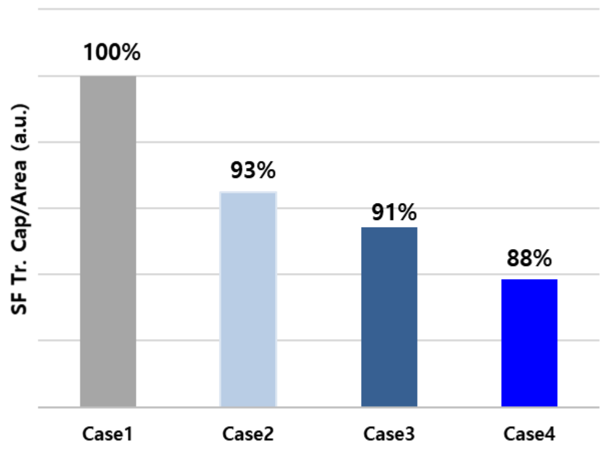

Figure 6. Comparison of ratio SF Tr. capacitance to area for each case

As seen in Figure 7, a reduction in drain width corresponds to improved low-signal linearity. This improvement in linearity is due to the decrease in drain area, which leads to a reduction in short-channel effects and enhances SF gain linearity. When extracting the value for linearity in a specific low-light signal region, the NDSF Tr. with the smallest drain width can reduce the low-light signal loss to 54% compared to the conventional SF Tr., as can be seen in Figure 8. In the case of NDSF Tr., the threshold voltage and SF gain remain similar, while DIBL is significantly reduced, as shown in Table 2.

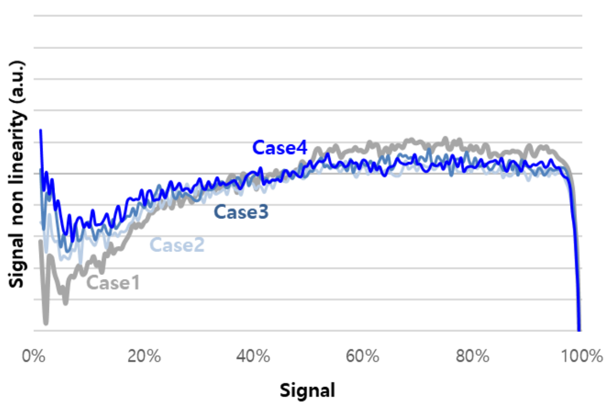

Figure 7. Relationship between SF capacitance and area

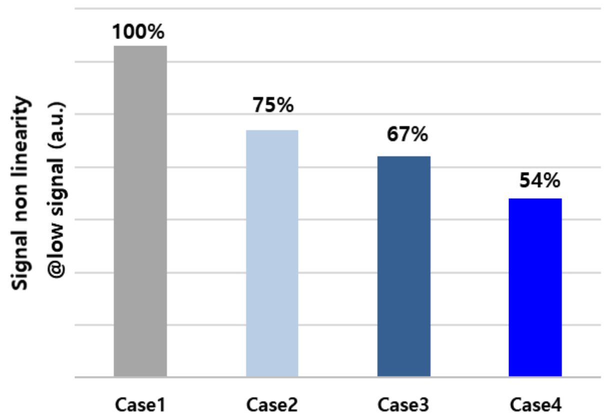

Figure 8. Comparison of ratio SF Tr. capacitance to area

	Case1	Case2	Case3	Case4
Vt @gmmax	100%	98%	98%	92%
SF Gain	100%	100%	100%	100%
DIBL	100%	75%	64%	50%

Table 2). Comparison of SF Tr. electrical characteristics measured by Test Element Group (TEG)

III. Conclusion

In conclusion, by adopting NDSF Tr., we significantly improve area efficiency and CG compared to conventional SF Tr. Additionally, enhancing short-channel effects improves signal non linearity in low-light signal region. These improvements contribute to a significant enhancement in low-light SNR and linearity in CIS, making NDSF Tr. a promising approach for advancing CIS performance.

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